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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,745	06/26/2003	Satoshi Kawasaki	67161-048	3806

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McDermott, Will & Emery
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Washington, DC 20005-3096

EXAMINER

LUU, PHO M

ART UNIT PAPER NUMBER

2824

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding..

Office Action Summary

Application No.

10/603,745

Applicant(s)

KAWASAKI, SATOSHI

Examiner

Pho M Luu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 3 is/are rejected.
- 7) ☒ Claim(s) 2 and 4-6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 6/26/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: Search History.

DETAILED ACTION

1. Claims 1-6 are pending in the application.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 26 June 2003. The information disclosed therein was considered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitsukawa et al. (US. 6,288,925).

Regarding claim 1, Kitsukawa et al. disclose, in Figures 1-2, 7a-7b and respective portion of the specification, a semiconductor memory (10, Fig. 1) device comprising:

a plurality of memory cell (array block of memory cell 12, Fig. 1) array regions arranged in matrix, space apart from each other in a row direction (16b, 16e, 16h, 16k, Fig. 1, see column 4, line 60) and in a column direction (16a, 16c, 16d, 16f, 16g, 16i, 16j, 16L, Fig. 1, see column 4, line 61) on a semiconductor substrate (inherence, a semiconductor device is implement substrate);

a plurality of sense amplifier (22a, 22b, 22c, Fig. 2) region each arranged in a gap between the memory array regions (array block of memory cell 12 in Fig. 1 contain the memory cell of the subarray 18a which is read only group of sense amplifier 22a, 22b in Fig. 2, also; see column 5, lines 23-25) in the column direction (16a, 16c, 16d, 16f, 16g, 16i, 16j, 16L, Fig. 1, see column 4, line 61) provided with a sense amplifier forming element;

a plurality of subdecoder (20a, 20b, 20c, 20d, Fig. 2) region each arranged in a gap between the memory cell array region (array block of memory cell 12 in Fig. 1 contain the memory cell of the subarray 18a which is selected the signal of subdecoders 20a, 20b in Fig. 2, also; see column 5, lines 19-21) in the row direction (16b, 16e, 16h, 16k, Fig. 1, see column 4, line 60);

a plurality of intersection region (24a, 24b, 24c, 24d, 24e, 24f, Fig. 2) each positioned at an intersection of the plurality of sense amplifier (22a, 22b, 22c, Fig. 2) regions in line and the plurality of subdecoder (20a, 20b, 20c, 20d, Fig. 2) region in line (see column 5, lines 28-30) and

a plurality of sense amplifier driver (sense amplifier 22a such as sense amplifier circuits 98a-98b in Fig. 7a, both connected to sense amplifier driver 100a, Fig. 7a, also;

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see column 8, lines 46-50) elements each arranged in the subdecoder region (subdecoder 20a generally be subdecoder circuit 106a-106d coupled to subdecoder driver 110a-110d in the intersection area 24a along with sense amplifier driver 100, Fig. 7b) for use in an operation of the sense amplifier.

With respected to claim 3, Kitsukawa et al. disclosed, in Fig. 1-2 and 7a-7b and respective portion of the specification, the semiconductor memory device (10, Fig. 1) which is the sense amplifier driver (100a, Fig. 7a) elements are dispersedly arranged in the subdecoder (106a-106d, Fig. 7b) and the intersection region (24a, Fig. 7b).

Allowable Subject Matter

6. Claims 2 and 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 2, the prior art of record do not disclose or suggest the subdecoder region adjacent to the end portion and a region on the outer side of the region provided with the plurality of memory cell array region.

Regarding claim 4, the prior art of record do not disclose or suggest a potential fixing conductor connected to the portion exposed in the subdecoder region for determining a potential of the conductive impurity diffusion region.

Regarding claim 5, the prior art of record do not disclose or suggest the sense amplifier are dispersedly arranged in two of the subdecoder regions positioned such that the intersection region adjacent to the one of the sense amplifier region is interposed therebetween.

Regarding claim 6, the prior art of record do not disclose or suggest the distances from boundary portion between the first conductivity type region and the second conductivity type region to the particular element are substantially equal.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakai et al. (US. 6,226,208) disclosed sub-sense amplifier signal is applied to the plurality of sense amplifier corresponding to each sub-array.

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for

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the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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08 June 2004



Pho M. Luu
Patent Examiner
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